AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for forming a transmission line structure for a semiconductor device, the method comprising:

forming an interlevel dielectric layer over a first metallization level;

removing a portion of said interlevel dielectric layer and forming a sacrificial material filled cavity within one or more voids created by the removal of said portion of said interlevel dielectric layer;

forming a signal transmission line in a second metallization level formed over said interlevel dielectric layer, said signal transmission line being disposed over said sacrificial material;

removing a portion of dielectric material, included within said second metallization level and adjacent each side of said signal transmission line so as to expose outer edges of said sacrificial material, wherein ~~a~~another portion of said sacrificial material is also exposed through a plurality of access holes formed through said signal transmission line; and

removing said sacrificial material so as to create an air gap beneath said signal transmission line.

2. (original) The method of claim 1, wherein said removing of said sacrificial material further results in a remaining support structure beneath said signal transmission line, said support structure comprising material from said interlevel dielectric layer.

3. (original) The method of claim 2, wherein said support structure further comprises a continuous rail.

4. (original) The method of claim 2, wherein said support structure further comprises a plurality of individual posts.

5. (original) The method of claim 1, further comprising forming a ground plane within said first metallization level, said ground plane further comprising a back end of line metallic material completely encapsulated within a liner material.

6. (currently amended) ~~The method of claim 5, further~~ comprising: A method for forming a transmission line structure for a semiconductor device, the method comprising:

forming a ground plane within a first metallization level, said ground plane further comprising a back end of line metallic material completely encapsulated within a liner material;

forming an interlevel dielectric layer over said first metallization level;

removing a portion of said interlevel dielectric layer and forming a sacrificial material filled cavity within one or more voids created by the removal of said portion of said interlevel dielectric layer;

forming a signal transmission line in a second metallization level formed over said interlevel dielectric layer, said signal transmission line being disposed over said sacrificial material;

forming a pair of coplanar shielding lines adjacent said signal transmission line in said second metallization level;

removing a portion of dielectric material included within said second metallization level so as to expose said sacrificial material, wherein a portion of said sacrificial material is exposed through a plurality of access holes formed through said signal transmission line; and

removing said sacrificial material so as to create an air gap beneath said signal transmission line.

7. (original) The method of claim 6, wherein said pair of coplanar shielding lines and said signal transmission line are also completely encapsulated with said liner material.

8. (original) The method of claim 6, further comprising forming vias in said interlevel dielectric layer for electrically connecting said pair of coplanar shielding lines and said ground plane.

9. (original) The method of claim 1, wherein said sacrificial material comprises an organic dielectric.

10. (original) The method of claim 9, wherein said sacrificial material is removed by a dry plasma etch.

11-30. (cancelled)